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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,977	09/17/2003	Hirohisa Tanabe	031794-3	1949

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EXAMINER	
YANCHUS III, PAUL B	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/663,977	TANABE ET AL.	
	Examiner	Art Unit	
	Paul B. Yanchus	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/17/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 4 is rejected under 35 U.S.C. 102(b) as being anticipated by Applicant's Admitted Prior Art [AAPA].

AAPA discloses an interface circuit provided for each of a first device set as a master side and a second device set as a slave side [two peripheral devices], for performing a serial data transmission between the first and second devices on the basis of a control signal [VBUS] which is output from the master side [page 1], comprising:

an oscillation circuit which generates a clock signal for data transmission upon receiving an operation-enable signal [master oscillator, page 2];

a transmission function portion which performs a serial data transmission with the other device upon receiving the clock signal [page 2];

a detection portion which monitors the control signal to output a detection signal when there is a change in the detection signal [detection circuit, page 2]; and

a process control portion which performs control of the operation-enable signal on the basis of the detection signal [page 2].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art [AAPA], in view of Kim, US Patent no. 6,845,454.

Regarding claim 1, AAPA discloses an interface circuit provided for each of a first device set as a master side and a second device set as a slave side [two peripheral devices], for performing a serial data transmission between the first and second devices on the basis of a control signal [VBUS] which is output from the master side [page 1], comprising:

a first oscillation circuit which generates a first clock signal for data transmission upon receiving an operation-enable signal [master oscillator, page 2];

a transmission function portion which performs a serial data transmission with the other device upon receiving the first clock signal [page 2];

a second clock signal having a frequency lower than that of the first clock signal [low-frequency clock, page 2]; and

a detection portion which detects the control signal on the basis of the second clock signal to output the operation-enable signal when a data transmission mode is designated by the control signal [detection circuit, page 2].

AAPA discloses using a master oscillator to generate both a first high frequency clock signal and a frequency divided low frequency clock signal for signal detection whilke in a low

power mode [pages 2 and 3]. AAPA does not disclose a second separate low power oscillator for generating the low frequency clock signal. Kim teaches using a first high frequency clock generator for generating a high frequency clock signal and a second low frequency clock generator for generating a low frequency clock signal instead of using a single high frequency for generating both of the high and low frequency clock signals [column 1, line 40 – column 2, line 23]. It would have been obvious to one of ordinary skill in the art to apply the Kim teachings to the AAPA interface circuit. Using a separate low frequency clock generator for generating a low frequency clock signal in a reduced power mode allows the high frequency clock generator to be disabled, which consequently reduces power consumption of the interface circuit [Kim, column 1, lines 57-61].

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art [AAPA] and Kim, US Patent no. 6,845,454, in view of Satou et al., US Patent no. 5,151,613 [Satou].

AAPA and Kim, as described above, disclose using a first high frequency clock generator for generating a high frequency clock signal and a separate second low frequency clock generator for generating a low frequency clock signal. AAPA and Kim are silent as to the types of clock generators that are used. However, as shown by Satou, CR oscillation circuits and quartz oscillation circuits are well known in the art. Satou discloses a clock supplying system, which outputs one of a clock signal generated by a CR oscillation circuit and a clock signal generated by a quartz [crystal] oscillation circuit. It would have been obvious to one of ordinary

skill in the art to use well known CR oscillation circuits and quartz oscillation circuits as the oscillation circuits in the AAPA and Kim interface circuit.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art [AAPA] and Kim, US Patent no. 6,845,454, in view of Watanabe, US Patent no. 6,473,477 and Dehghan, US Patent no. 6,275,087.

AAPA and Kim, as described above, disclose a detection portion, which detects the control signal on the basis of the second clock signal to output the operation-enable signal when a data transmission mode is designated by the control signal. AAPA and Kim are silent as to the specific components that are inside the detection portion and therefore do not explicitly disclose a shift register which shifts and holds the control signal and a noise removal circuit for removing noise components from the control signal. However, as shown by Watanabe [column 17, lines 50-54], using shift register circuitry in signal detection circuits is well known in the art and as shown by Dehghan [column 6, lines 40-52], using noise removal circuitry in signal detection circuits is well known in the art. It would have been obvious to one of ordinary skill in the art to use well known shift register and well known noise removal circuitry in the AAPA and Kim detection portion of the interface circuit.

Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art [AAPA].

AAPA, as described above, discloses a detection portion, which monitors the control signal to output a detection signal when there is a change in the detection signal. AAPA is silent as to the specific components that are inside the detection portion.

Applicant(s) numerous definitions of the internal circuitry of the detection portion (claims 5-7) is construed to be an admission that the criticality does not reside in the type of internal circuitry utilized in the detection portion and hence are obvious variations of one another.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art [AAPA], in view of Dehghan, US Patent no. 6,275,087.

AAPA, as described above, discloses a detection portion, which monitors the control signal to output a detection signal when there is a change in the detection signal. AAPA is silent as to the specific components that are inside the detection portion. AAPA is silent as to the specific components that are inside the detection portion and therefore do not explicitly disclose a noise removal circuit for removing noise components from the control signal. However, as shown by Dehghan [column 6, lines 40-52], using noise removal circuitry in signal detection circuits is well known in the art. It would have been obvious to one of ordinary skill in the art to use well known noise removal circuitry in the AAPA detection portion of the interface circuit.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Adduci, US Patent no. 5,621,361 discloses using a crystal oscillator that comprises a quartz oscillator.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B. Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Yanchus
February 19, 2006

LYNNE H. BROWNE
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